Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: Au**

**S = .003” X .003”**

**G = .003 X .006”**

**D = .003 X .003”**

**Substrate is GATE**

**Mask Ref: 5021**

**APPROVED BY: DK DIE SIZE .016” X .019” DATE: 4/27/23**

**MFG: CALOGIC THICKNESS .005” P/N: U308 / U309 / U310**

**DG 10.1.2**

#### Rev B, 7/1